G.PULLA REDDY ENGINEERING COLLEGE (Autonomous) :: KURNOOL

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TIME TABLE for the Academic year 2023-2024 with effect from 01-11-2023

VLSI & Embedded Systems(VLSI & ES)

CLASS : M.Tech - I semester(Scheme-2022) **LECTURE HALL: PG4**

Day / Time	09.30 am - 10.30 am	10.30 am -11.30am	11.45 am - 12.45pm		1.30 pm - 2.30pm	2.30 pm - 3.30pm	3.30 pm - 4.30pm
MON	ADSD gvrs	ESA gr	DVD dro	LUNCH BREAK	VTECH mmsr	ERPW asn	
TUE	DVD dro	VTECH mmsr	AES smsd		AES Lab smsd,gr		
WED	RM kr	ESA gr	AES smsd		ADSD gvrs	LIB	LIB
THU	AVLSI Lab mmsr,gdp						
FRI	AES smsd	ESA gr	ADSD gvrs		DVD dro	VTECH mmsr	RM kr
SAT							

		Theory:			Faculty Member:
1	DVD	Digital VLSI Design	---------	dro	Smt D. Rohini
2	AES	Advanced Embedded Systems		smsd	Dr .S.M.Shamsheer Daula
3	ADSD	Advanced Digital System Design Using Verilog	---------	gvrs	Dr G.V.R Sagar
4	VTECH	VLSI Technology (Professional Elective-I)	---------	mmsr	Sri.M.Madhu Sudhan Reddy
5	ESA	Embedded System Architecture (ESA) (Professional Elective-II)	---------	gr	Dr G. Ramesh
6	RM&IPR	Research Methodology & IPR	---------	kr	Sri K. Raju
7	ERPW(AC-1)	Audit Course - I (English for research Paper Writing)	---------	as	Ms..A. Srinidhi
	Practicals				
8	AVLSIL	Advanced VLSI Lab	---------	mmsr	Sri.M.Madhu Sudhan Reddy, Smt G. Divya Praneetha
9	AESL	Advanced Embedded Systems Lab	---------	smsd	Dr .S.M.Shamsheer Daula,Dr G. Ramesh

Prepared by : Sri B. Siva Reddy **Verfied by: HOD (E.C.E.)** **Approved by :PRINCIPAL**